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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/686,323	10/09/2000	Bin Zhao	97RSS433DIV	6870

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EXAMINER	
PERALTA, GINETTE	
ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

11-A

Office Action Summary	Application No.	Applicant(s)	
	09/686,323	ZHAO, BIN	
	Examiner	Art Unit	
	Ginette Peralta	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *93-101,104-113,116 and 117* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *93-99,104-109,116 and 117* is/are rejected.

7)☒ Claim(s) *100-101,110-113* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 93-99, 104-109, and 116-117 are rejected under 35 U.S.C. 103(a) as being unpatentable over Michael et al. in view of Chen et al. and Grill et al. (U. S. Pat. 6,017,814).

Michael et al. discloses in col. 5, line 10-col. 7, line 57, a method of manufacturing an interconnect that comprises forming a first patterned layer of conductive material 11, the first patterned layer having at least one trench situated between a first and a second interconnect line; depositing a first insulating layer 20 over the first patterned layer 11, the insulating layer filling the at least one trench; forming a first air gap, a second air gap, and a support pillar in the first insulating layer 20, the support pillar being situated between the first air gap and the second air gap (figs. 6 and 7), the support pillar, the first air gap, and the second air gap being situated in the trench, it is further taught that a support pillar is in contact with the first interconnect line (as shown in fig. 6) when other gaps are formed in the structure; depositing a sealing layer over the first

insulating layer to seal the first air gap and the second air gap, wherein the first insulating layer of Michael et al. comprises silicon oxide.

Michael et al. discloses the claimed invention with the exception of depositing a first hard mask on the first insulating layer and forming the first air gap, the second air gap and the support pillar on the first hard mask, and the support pillar, the first air gap, and the second air gap being situated in a trench in a direction parallel to a length of the first interconnect line and the first insulating layer and the sealing layer comprising a low dielectric constant material.

Chen et al. discloses in col. 3, line 36- col. 4, line 13 a method of manufacturing an interconnect that comprises depositing a first insulating layer 24 over the substrate 20; depositing a first hard mask 26 on the first insulating layer; and forming a trench in the first hard mask and the first insulating layer; wherein the first insulating layer 24 comprises a low-k dielectric material used as a replacement for silicon oxide; wherein the use of a spin-on organic polymer has the effect of improving the planarization of the wafer surface, and in order to further improve performance of the integrated circuits(col. 1, ll. 26-46), and the first hard mask is used to protect the low-k dielectric material that may exhibit patterning problems because of their low etch rate selectivity with respect to photoresist(col. 1, ll. 47-56); and furthermore since the utilization of a hardmask permits the use of very thin photoresist layers to pattern the hardmask, a requirement for the resolution of images by deep ultraviolet photolithography (col. 4, lines 4-13).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a low-k dielectric material as the first insulating layer for the disclosed intended purpose of Chen et al. that the use of a spin-on organic polymer has the effect of improving the planarization of the wafer surface (col. 3, lines 62-67), and in order to further improve the performance of the integrated circuits (col. 1, ll. 26-46), and to deposit a first hard mask over the first insulating layer for the disclosed intended purpose of protecting the first insulating layer that may exhibit patterning problems because of their low etch rate selectivity with respect to photoresist, and furthermore since the utilization of a hardmask permits the use of very thin photoresist layers to pattern the hardmask, a requirement for the resolution of images by deep ultraviolet photolithography (col. 4, lines 4-13). Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the hardmask layer over the first insulating layer and then forming a first air gap, a second air gap, and a support pillar in the first hard mask and the first insulating layer for the disclosed intended purpose of Chen et al. of aiding in the use of very thin photoresist layers to form patterns that require very high resolution as is the case and as taught in col. 4, lines 4-13.

Grill et al. discloses a method of manufacturing an interconnect in which as shown in figs. 3-5, a first patterned layer of conductive material 7 is formed, the first patterned layer having a trench situated between a first and a second interconnect line; and forming a first air gap 5, a second air gap 5, and a support pillar 4 in the first

insulating layer, the support pillar being situated between the first air gap and the second air gap, the support pillar, the first air gap, and the second air gap being situated in the trench in a direction parallel to a length of the first interconnect line, the support pillar being in contact with the first interconnect line, and the support pillar being formed to increase mechanical strength and thermal conductivity of the first interconnect line, wherein the first air gap, the second air gap, and the support pillar are situated in a trench in a direction parallel to the length of the first interconnect line, and the support pillar is in contact with the interconnect line for the disclosed intended purpose of personalizing the patterned dielectric structures in order to minimize the dielectric constant of the insulating material as taught in col. 2, line 66 to col. 3, line 17.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first air gap, the second air gap, and the support pillar situated in a trench in a direction parallel to the length of the first interconnect line, and the support pillar is in contact with the interconnect line for the disclosed intended purpose of personalizing the patterned dielectric structures in order to minimize the dielectric constant of the insulating material, as Grill et al. teaches that this is personalization of the insulating layer and it would have been obvious to one of ordinary skill in the art as taught in col. 2, line 66 to col. 3, line 17.

With regards to the feature of the sealing layer and the insulating layer comprising a low dielectric constant material, Michael et al. discloses the use of silicon oxide for the sealing layer, Chen et al. discloses that low dielectric constant materials are

being used as alternatives for silicon oxide in order to improve the performance of the integrated circuits. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a low dielectric constant material as the sealing layer in the invention of Michael et al. for the disclosed intended purpose of Chen et al. of improving the performance of the integrated circuit and in accordance with Michael et al.'s disclosed intended purpose of providing a dielectric fabrication process that produces a low permittivity between the interconnect lines.

With regards to the feature of applying a photoresist material to the first hard mask and etching the first and second air gap in the first hard mask and the first insulating layer, Michael et al. discloses in col. 6, ll. 10-32, that the step of forming a first air gap and a second air gap comprises a masking step and an etching, and Chen et al. discloses that the first hardmask is used for the disclosed intended purpose of enhancing the resolution of the patterning of the dielectric layer when using a photoresist layer.

With regards to the feature of opening a via hole in the sealing layer, the first hard mask, and the first insulating layer, Michael et al. discloses in fig. 12 that the method further comprises opening a via hole 46 in the sealing layer and the first insulating layer. Michael et al. as modified by Chen et al. would teach that the via hole 46 is also formed in the first hard mask and as further disclosed by Chen et al. that the dielectric layer is patterned in conjunction with the hard mask material with an enhanced resolution over using the dielectric layer alone as taught in col. 4, lines 4-13.

With regards to the feature of the steps of forming the via hole, Michael et al. discloses in col. 7, ll. 19-52, that in order to open the via hole in the sealing layer, and the first insulating layer a trench mask is applied defining a via hole pattern, and etching a via hole in the sealing layer and the first insulating layer based on the via hole pattern.

With regards to the feature of forming a conductive plug and forming a second patterned conductive layer, Michael et al. discloses that a conductive plug is formed in the via hole 46; and also teaches in col. 7, lines 30-67, forming a second patterned layer 40 of conductive material over the sealing layer 30.

With regards to the feature of depositing a second insulating layer over the first insulating layer; prior to forming the air gaps, it is noted that in col. 6, lines 1-2, that the dielectric 20 could be deposited by depositing the layer in two or more stages, wherein each deposition is followed by a planarization step for the disclosed intended purpose of obtaining a substantially planar surface.

With regards to the feature of the conductive material, Michael et al. discloses that the first patterned layer of conductive material comprises aluminum.

Allowable Subject Matter

3. Claims 100, 101, and 110-113 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

4. Applicant's arguments filed 12/7/04 have been fully considered but they are not persuasive.

With regards to applicant's argument that Michael fails to teach or remotely suggest a first insulating layer and a sealing layer that comprise a low dielectric constant material, it is noted that Michael discloses the use of a TEOS based oxide as the first insulating layer and that the purpose of etching trenches in the first insulating layer is for the purpose of lowering the permittivity between the interconnect lines as disclosed in col. 2, lines 54-60, it is further noted that the permittivity of the material is characterized by the dielectric constant, and that Chen et al. discloses the use of a low dielectric constant material as an alternative to silicon oxide in order to further improve performance by producing interconnective wiring that complies with the restrictive RC time constraints of devices having higher densities (col. 1, lines 26-46). Thus the use of low constant dielectric would be an obvious modification of Michael as taught by Chen as it further improves the structure of Michael by lowering even further the permittivity between the interconnect lines of Michael et al..

With regards to applicant's argument that Michael fails to teach, disclose or suggest forming a support pillar between air gap trenches 26 where the support pillar is in contact with an interconnect line, and where the support pillar is formed to increase the mechanical strength and thermal conductivity of the interconnect line, it is noted that Michael et al. discloses in Fig. 6 support pillars that are in contact with the

interconnect line, and that the location of the support pillars inherently increase the mechanical strength and the thermal conductivity of the interconnect line by increasing the effective surface of the interconnect line.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (571)272-1713. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GP

DOUGLAS WILLE
PRIMARY EXAMINER